PATENT ABSTRACTS OF JAPAN

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(54) INSTRUCTION DESIGNATION SYSTEM AND INSTRUCTION EXECUTION SYSTEM

(57)Abstract:

PURPOSE: To improve bit use efficiency by forming a large instruction word by means of a specified instruction word and a type code designating the structure and designating one or plural instructions which are executed in parallel by means of the large instruction word.

CONSTITUTION: The large instruction word is constituted of the type code and the instruction word, and the instruction word has at least an instruction code and an operand designation part so as to designate a signal instruction. When the large instruction word consists of 64 bits, bits 0-3 are set to be the type codes, and bits 4-23, 24-43 and 44-63 to the three instruction words of a system A. Furthermore, the instruction words of the system A consist of the instruction code OPa of five bits, the first register designation field Ra1 of five bits as the operand designation part, a second register designation field Ra2 and a third register designation field Ra3. Then, one or plural instructions which are executed in parallel

by one large instruction word can be designated.

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